AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) In an electronic system, a system for voltage margin testing of one or more components of said system, comprising:

a Baseboard Management Controller (BMC) that implements an Intelligent Platform Management Interface (IPMI) protocol, the BMC-internal to said electronic system; and

a digital voltage adjuster configured to communicate with said controller and to affect generation of one or more test voltages for application to said one or more components in response to commands from the controller.

2. (Previously Presented) The margin testing system of claim 1, further comprising:

diagnostics software capable of collecting and analyzing data regarding a response of said system to said test voltages.

3. (Original) The margin testing system of claim 1, further comprising:

a power rail electrically coupled to said components for applying voltage thereto, said voltage adjuster being electrically coupled to said power rail to set said power rail voltage to one or more of said test voltages.

4. (Previously Presented) The margin testing system of claim 3, further comprising:

a voltage regulator configured to receive an input voltage and generate a regulated output voltage for application to said power rail, said voltage adjuster being coupled to said regulator for varying said regulated output voltage in response to commands from said controller.

5. (Previously Presented) The margin testing system of claim 4, wherein said digital voltage adjuster comprises:

a digital potentiometer incorporated in a feedback circuitry of said voltage regulator,

wherein the digital potentiometer is configured to vary a resistance associated with said feedback circuitry in response to commands from said controller so as to vary said output voltage of the regulator.

6. (Previously Presented) The margin testing system of claim 4, further comprising:

a hardware monitor in communication with said regulator and said controller, said hardware monitor configured to measure said output voltage of said regulator and transmit said measured voltage to said controller.

7. (Previously Presented) The margin testing system of claim 6, wherein said controller is further configured to query said hardware monitor periodically to receive said measured voltage and wherein, said controller is further configured to transmit a feedback command to said adjuster based on said measured voltage to cause the adjuster to vary the output voltage of the regulator from said measured value to a selected test value.

8. (Canceled)

9. (Canceled)

10. (Previously Presented) The margin testing system of claim 1, further comprising:

an Inter-Integrated Circuit (I^2C) based bus for providing communication between said BMC and said voltage adjuster.

11. (Previously Presented) The margin testing system of claim 1, wherein said controller is configured to initiate margin testing in response to a command from an external system.

12. (Original) The margin testing system of claim 1, wherein said electronic system comprises:

a computer system.

13. (Original) The margin testing system of claim 12, wherein said computer system is a server.

14. (Previously Presented) A computer system, comprising:

a processor;

a plurality of components in communication with said processor for performing a plurality of tasks;

a Baseboard Management Controller (BMC) that implements an Intelligent Platform Management Interface (IPMI) protocol; and

a digital voltage adjuster configured to communicate with said controller affect generation of one or more test voltages for application to selected ones of said components for voltage margin testing thereof in response to commands from said controller.

15. (Canceled)

16. (Previously Presented) The computer system of claim 14, further comprising:

an Inter-Integrated (I^2C) based bus for providing communication between said BMC and said voltage adjuster.

17. (Previously Presented) The computer system of claim 14, further comprising:

a voltage regulator configured to receive an input voltage and generate a regulated output voltage for application to said components.

18. (Previously Presented) The computer system of claim 17, wherein said voltage adjuster comprises:

a digital potentiometer incorporated in a feedback circuitry of said voltage regulator said digital potentiometer configured to vary a resistance of said feedback circuitry in response to commands from said controller in order to set the output voltage of said regulator to one or more of said test voltages.

19. (Previously Presented) A method for voltage margin testing of one or more components of an electronic system, having an internal Baseboard Management Controller (BMC) that implements an Intelligent Platform Management Interface (IPMI) protocol and a digital voltage adjuster, the digital voltage adjuster in communication with said BMC and with at least a power rail supplying voltage to said components, comprising:

the BMC transmitting one or more commands to said voltage adjuster to cause the adjuster to affect generation of one or more test voltages at said power rail; and

monitoring said computer system to determine a response to each of said test voltages.

20. (Previously Presented) The method of claim 19, wherein said controller is a Baseboard Management Controller (BMC).

21. (Previously Presented) The method of claim 20, further comprising:

employing an Inter-Integrated Circuit (I^2C) based bus for providing communication between said BMC and said voltage adjuster.

22. (Previously Presented) The method of claim 19, wherein monitoring said computer system to determine a response comprising:

a hardware monitor measuring a voltage at said power rail and transmitting said measured voltage to said controller.

23. (Currently Amended) In an electronic system, a system for voltage margin testing of one or more components of said system, comprising:

a controller internal to said electronic system; and

a digital voltage adjuster configured to communicate with said controller and to affect generation of one or more test voltages for application to said one or more components in response to commands from the controller; and

a voltage regulator configured to receive an input voltage and generate a regulated output voltage for application to a power rail, said voltage adjuster being coupled to said regulator for varying said regulated output voltage in response to commands from said controller; and

a hardware monitor in communication with said regulator and said controller, said hardware monitor configured to measure said output voltage of said regulator to determine a measurement value and transmit said ~~measured voltage~~ measurement value to said controller.

24. (Currently Amended) The margin testing system of claim 23, wherein said controller is further configured to query said hardware monitor periodically to receive said measurement value ~~measured voltage~~ and wherein, said controller is further configured to transmit a feedback command to said adjuster based on said measurement value ~~measured voltage~~ to cause the adjuster to vary the output voltage of the regulator from said measurement value ~~measured value~~ to a selected test value.

25. (Previously Presented) The margin testing system of claim 23, wherein said controller is a Baseboard Management Controller (BMC).

26. (Previously Presented) The margin testing system of claim 25, wherein said BMC implements Intelligent Platform Management Interface (IPMI) Protocol.

27. (Previously Presented) A system for voltage margin testing of one or more components of an electronic system, comprising:

means for transmitting one or more commands to a means for adjusting a voltage to cause the means for adjusting to affect generation of one or more test voltages at a power rail supplying voltage to said components, the means for transmitting implementing an Intelligent Platform Management Interface (IPMI) protocol; and

means for monitoring said computer system to determine a response to each of said test voltages.